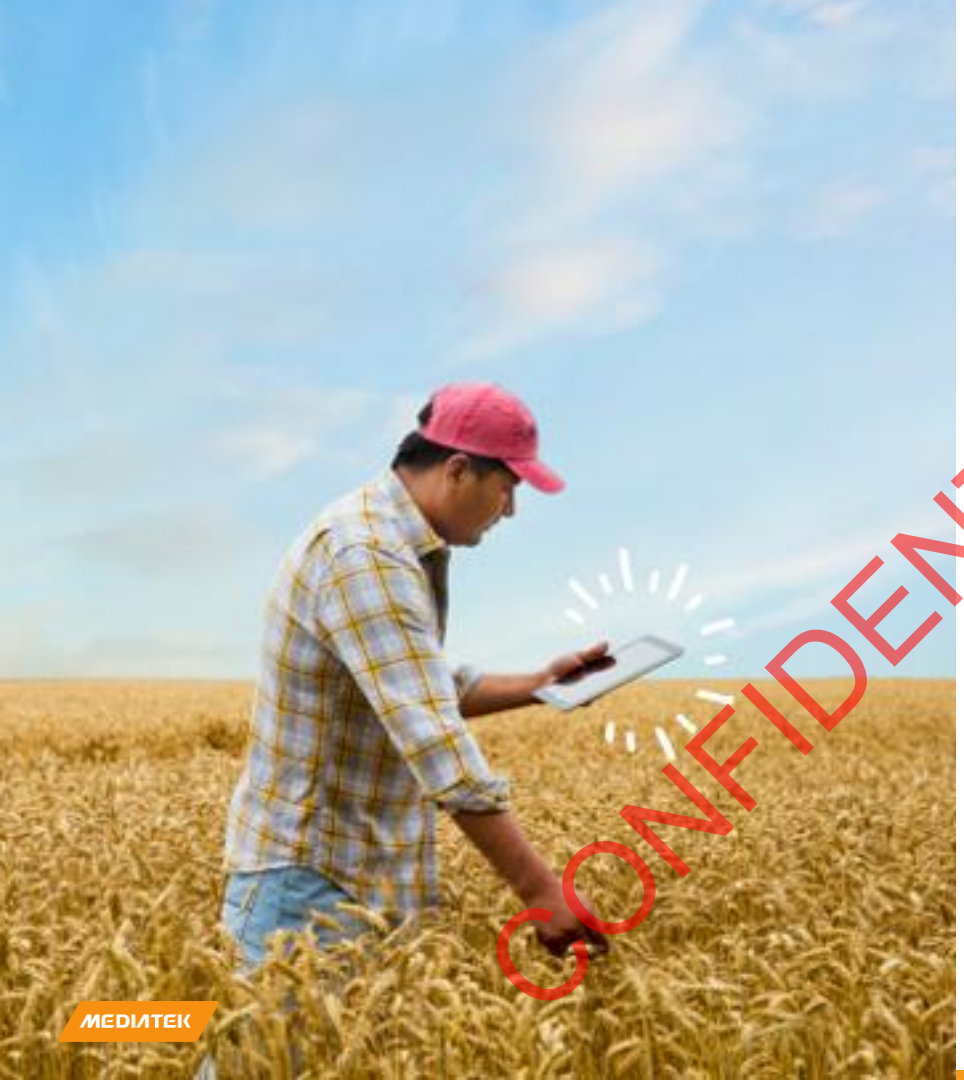
WE'RE A GROWING GLOBAL TECHNOLOGY COMPANY WITH A CLEAR VISION FOR THE FUTURE



BY BUILDING TECHNOLOGIES THAT HELP CONNECT INDIVIDUALS TO THE WORLD AROUND THEM, WE ARE ENABLING PEOPLE TO EXPAND THEIR HORIZONS AND MORE EASILY ACHIEVE THEIR GOALS.

Habilitamos mas de 1 Billón de dispositivos por año

#3	#1	#1	#2	#1	#1	#1
Connectivity network	Feature phone	Tablet	Smartphone	Digital TV*	DVD/BD player	Optical disc drive

Source (ranking by revenue of 2015): Strategy Analytics, Gartner, IDC, IC Insight, iSuppli and MediaTek company data
* Combined with MStar. Source (Rankings by volume): Strategy Analytics, Displaysearch, iSuppli , MediaTek company data

3era Compañía Fabless SoC en el Mundo

Ranking	Company	H1 2015 Revenue (US$ M)
1	Qualcomm	8,287
2	Avago+Broadcom	7,465
3	**MediaTek**	**3,032****
4	NVidia	2,118
5	AMD	1,972

Source: IC Insight's Strategic Reviews database (August 2015) , company reports. All data based on 2015 calendar year's first half.
*Broadcom and Avago are expected to consolidate in 16'Q1, pro-forma revenue is used for this table.
** Revenue calculation is based on IC Insight's data and varies slightly from MediaTek's actual revenue (as of Q3 2015).

Un Viaje de 19 años

1997

70 Empleados - Taiwan

Unico Producto - CDROM

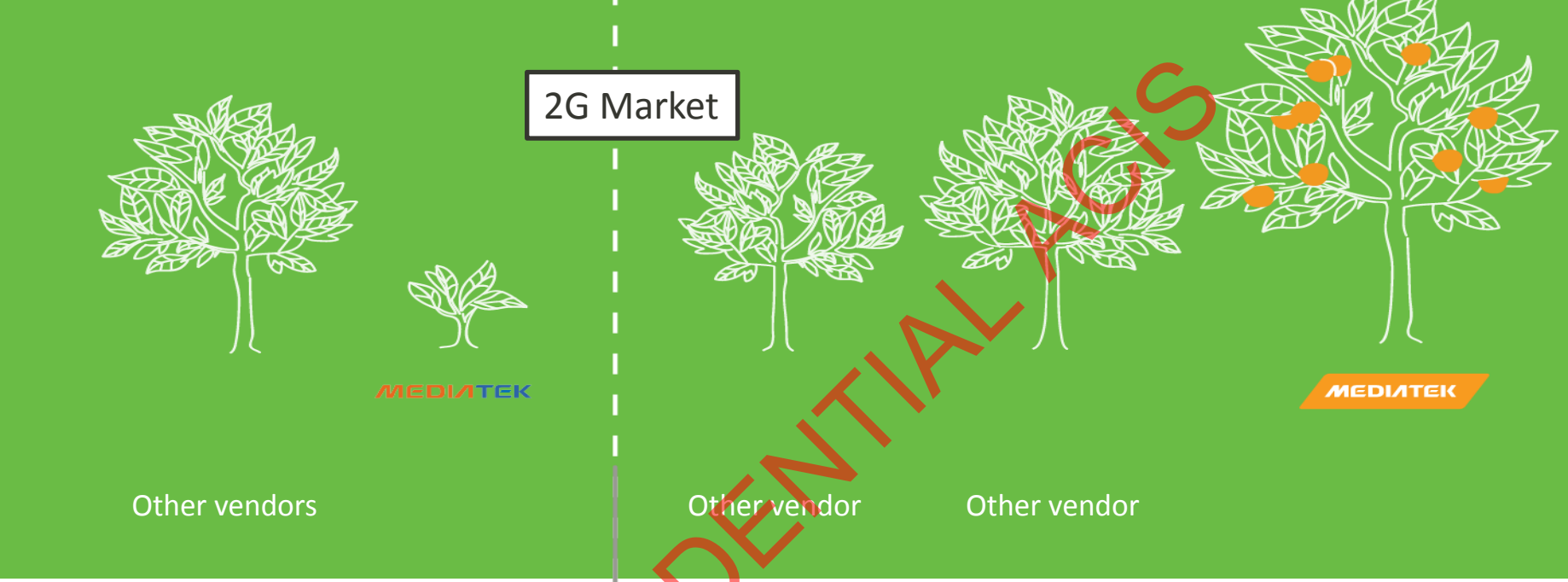
Ventas USD < $25M

2016

12,000 Empleados - A nivel Mundial

Línea Completa de Chipsets
- No. 1 Digital TV, BD/Theater
- No. 2 Mobile Phone/Tablet
- No. 1 PC Optical Drive
- Connectivity, Wearable, IoT, …

Ventas +USD $7,000M



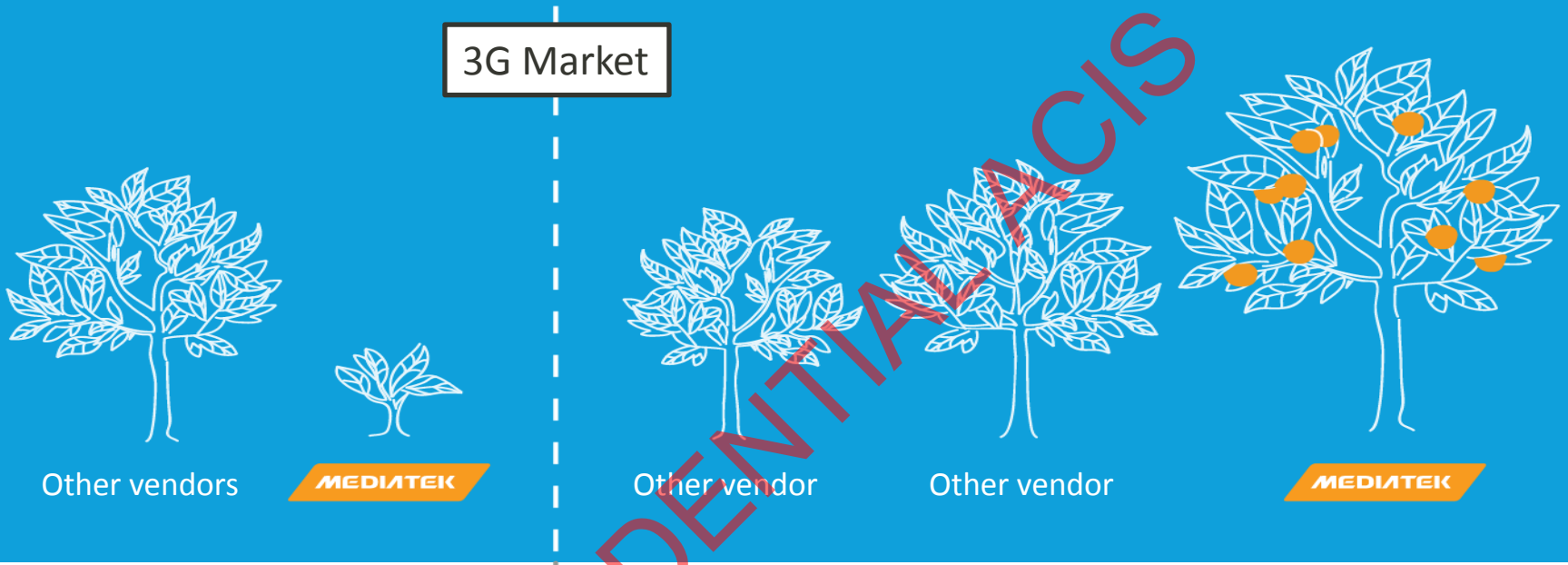
2004

MediaTek Lanza su primer producto 2G

6 años

2010

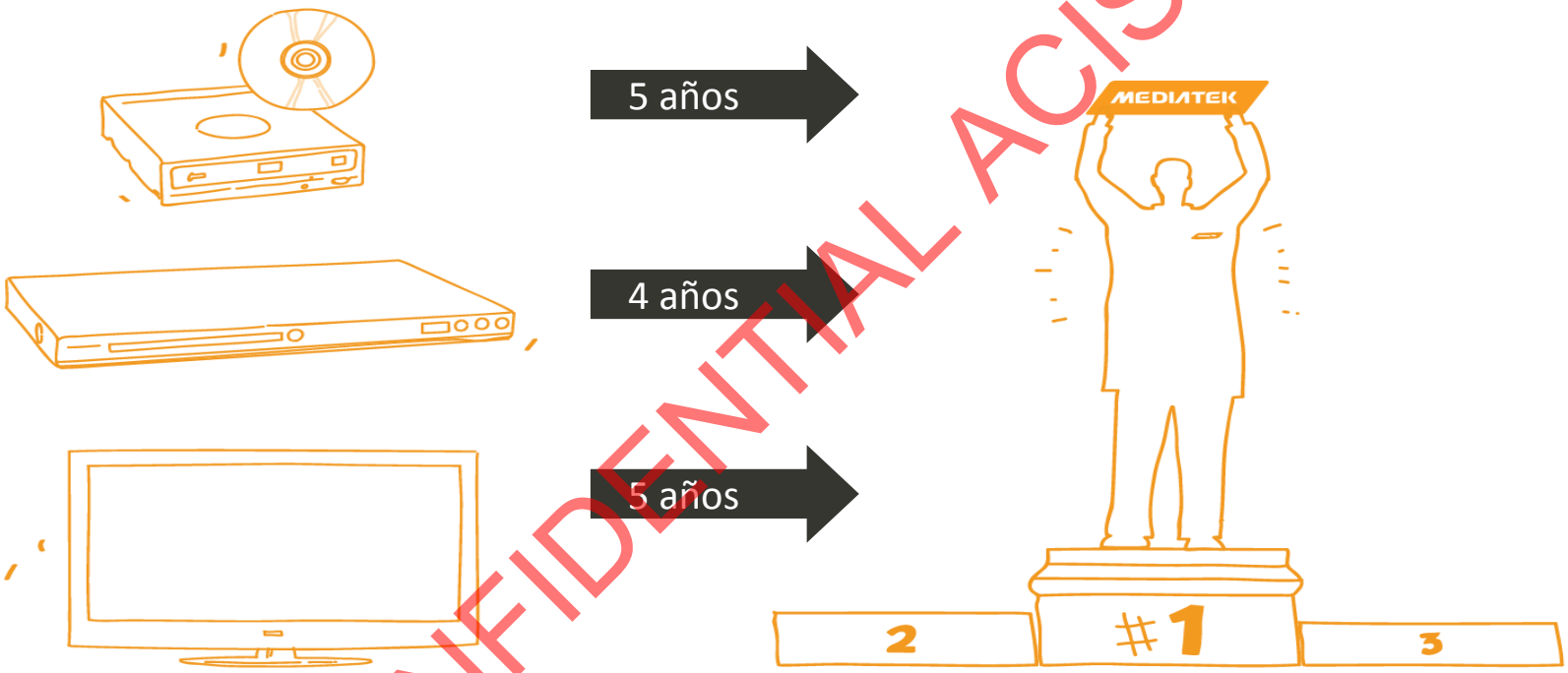
#1 en Market Share Mundial de 2G



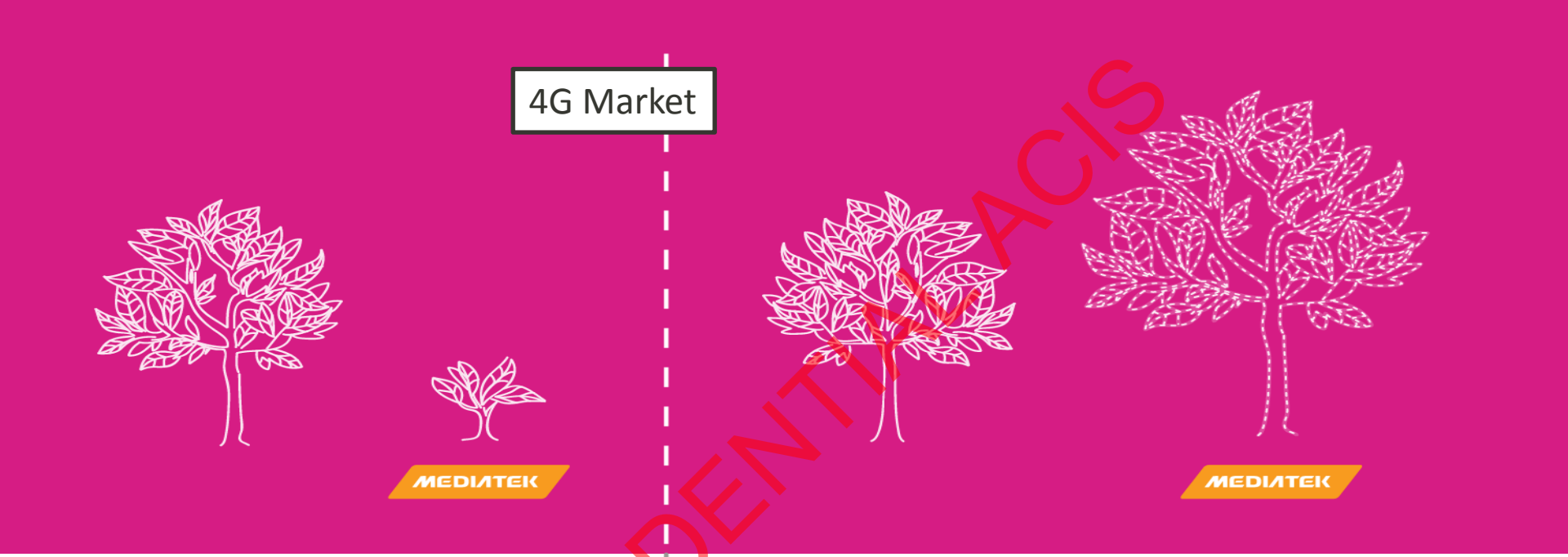
2010
MediaTek Lanza su Primer Producto 3G

4 años

2014
#1 Market Share Mundial en**3G**



No Solo en la Industria movil

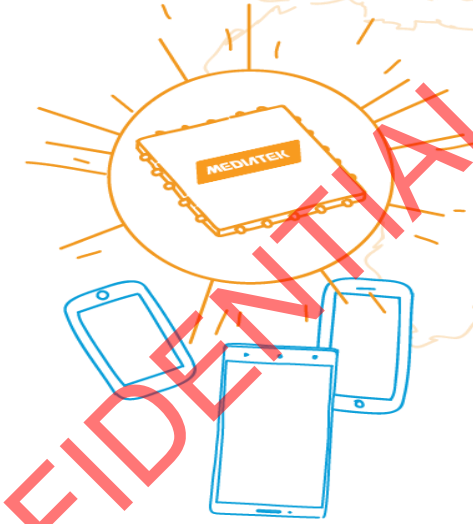


2014

MediaTek Lanza su Primer Chipset 4G

#1 ?

1 in 3 phones is MediaTek based (2015)



2015 Global Mobile Phone Shipment (Feature Phone + Smartphone)

MediaTek > 650million, including > 40m LTE

Global 1.8~1.9 billion

Source: Strategy Analytics (September 2014), MediaTek

Presencia Global

Total empleados:

12,000+

Reconocimiento como Líder Tecnológico

- Featured in Thomson Reuters *Top 100 Global Innovators* for 2nd year in a row
- Ming-Kai Tsai, Chairman & CEO receives the 2015 *Dr. Morris Chang Exemplary Leadership Award* from the GSA
- Fourth consecutive *Outstanding Asia Pacific Semiconductor Company Award* by the Global Semiconductor Alliance (GSA)

GSA
2015 AWARDS
WINNER

Clientes Ejemplares

HUAWEI TOSHIBA ALCATEL onetouch LG NOKIA hp Telefónica Pioneer GENERAL MOBILE

lenovo Panasonic BLU azumi b mobile b connected wolder Haier LANIX vivo ARCHOS SAMSUNG

ZTE中兴

ASUS

arçelik

acer

mycromax

oppo

htc Microsoft SONY amazon

One M9+

XBOX

Xperia M5

Fire HD Tablets

NETGEAR

GARMIN

VIZIO

D-Link

TCL

YAMAHA

COMCAST

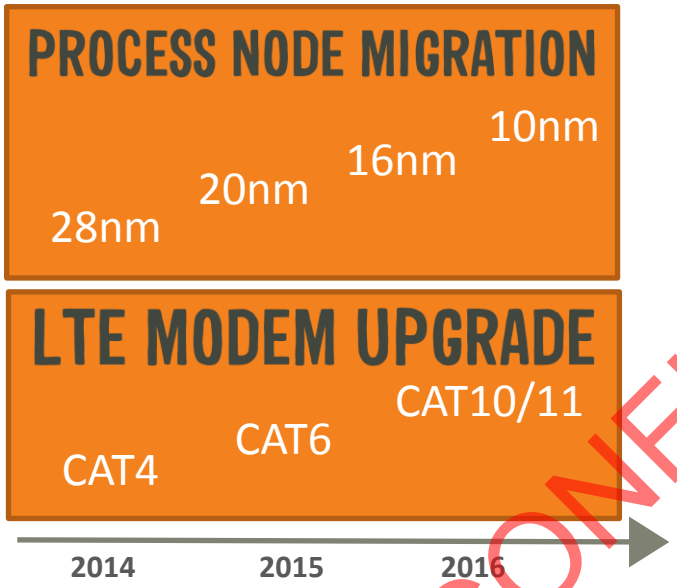
verizon verykool ENERGY SISTEM TECNO Mobile LAVA bq Wiko MTS INNJOO yezz MYWIGO SMARTPHONES CISCO

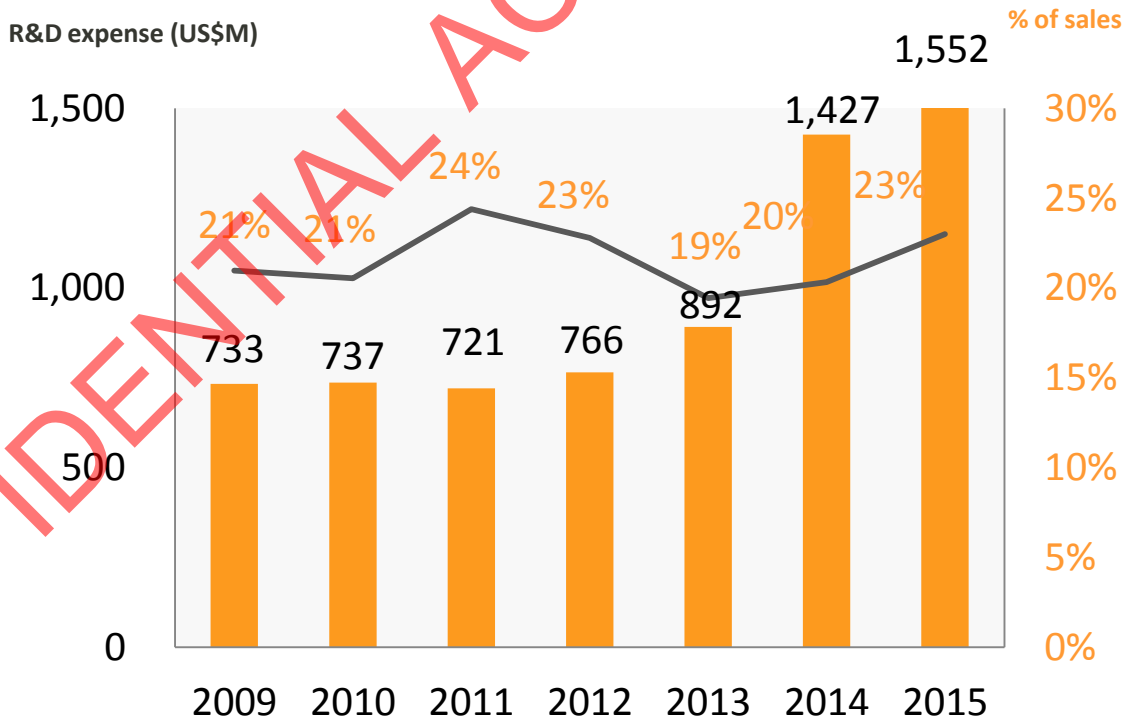
VESTEL at&t T··Mobile· vodafone orange 中国移动 China Mobile China unicom中国联通 EE Telit SIERRA WIRELESS Beeline gemalto

MEDIATEK

Como Lo Logramos?

Gran Inversión en R&D





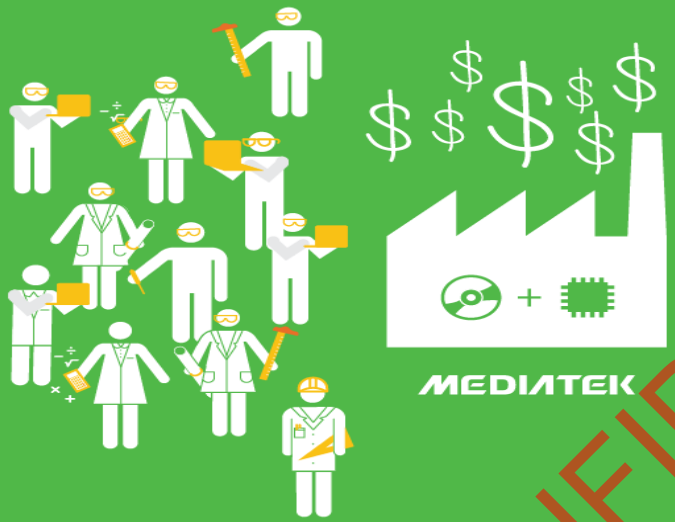
MEDIATEK

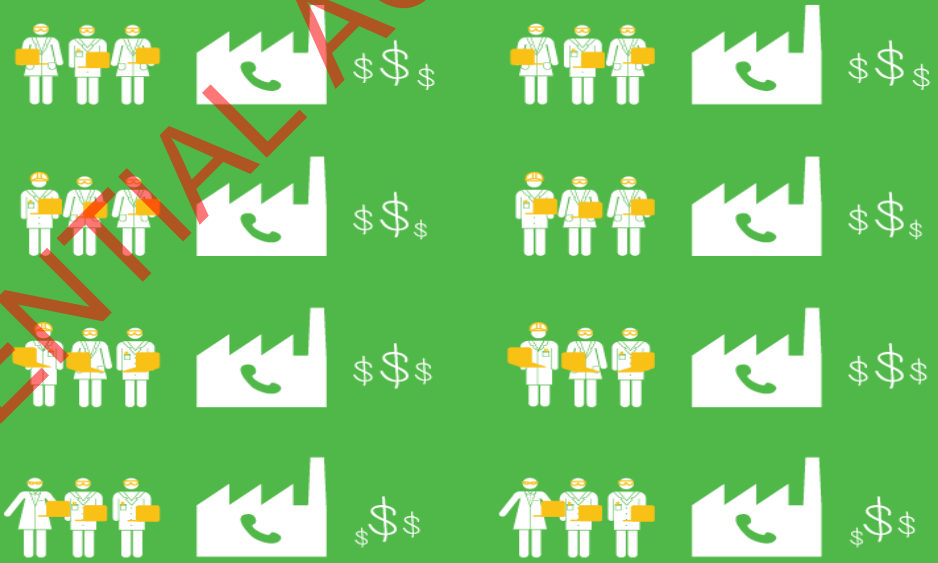
Before

Duplication of R&D

MEDIATEK

After





R&D Resource
Efficiency and Scale

La Visión de MediaTek

Creemos en que cada uno de nosotros puede conseguir algo espectacular, también si lo es en un hecho pequeño.
Y creemos que es posible hacerlo todos los días.
Llamamos esta idea
Everyday Genius *(Genio en*

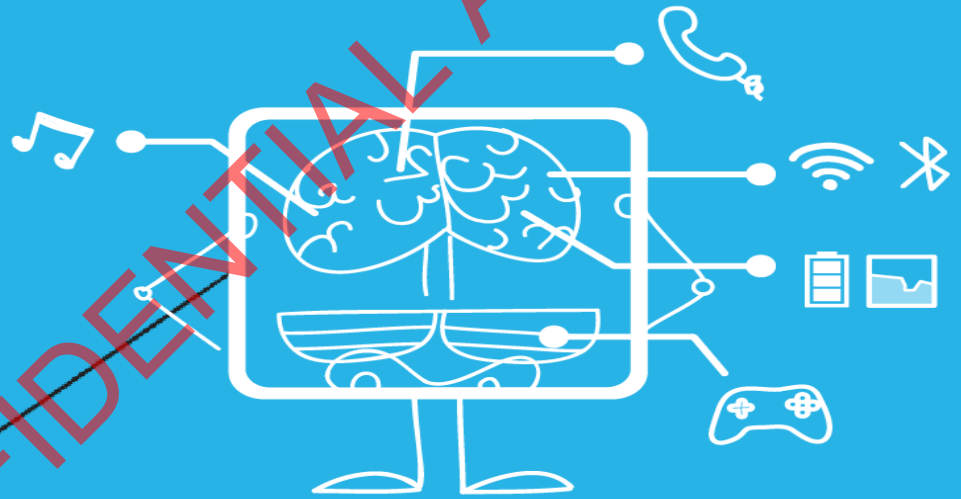
todo momento) y todo lo que

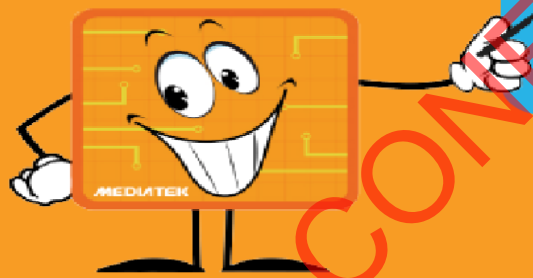
hacemos esta dedicado a
que sea posible.

http://youtu.be/k2tPgEwqz6s

MEDIATEK

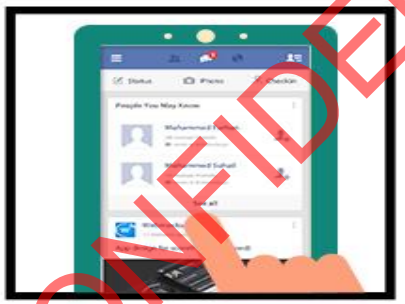
QUE ES UN SoC?





Las Necesidades del Ser Humano

EXPERIENCIA DE USUARIO

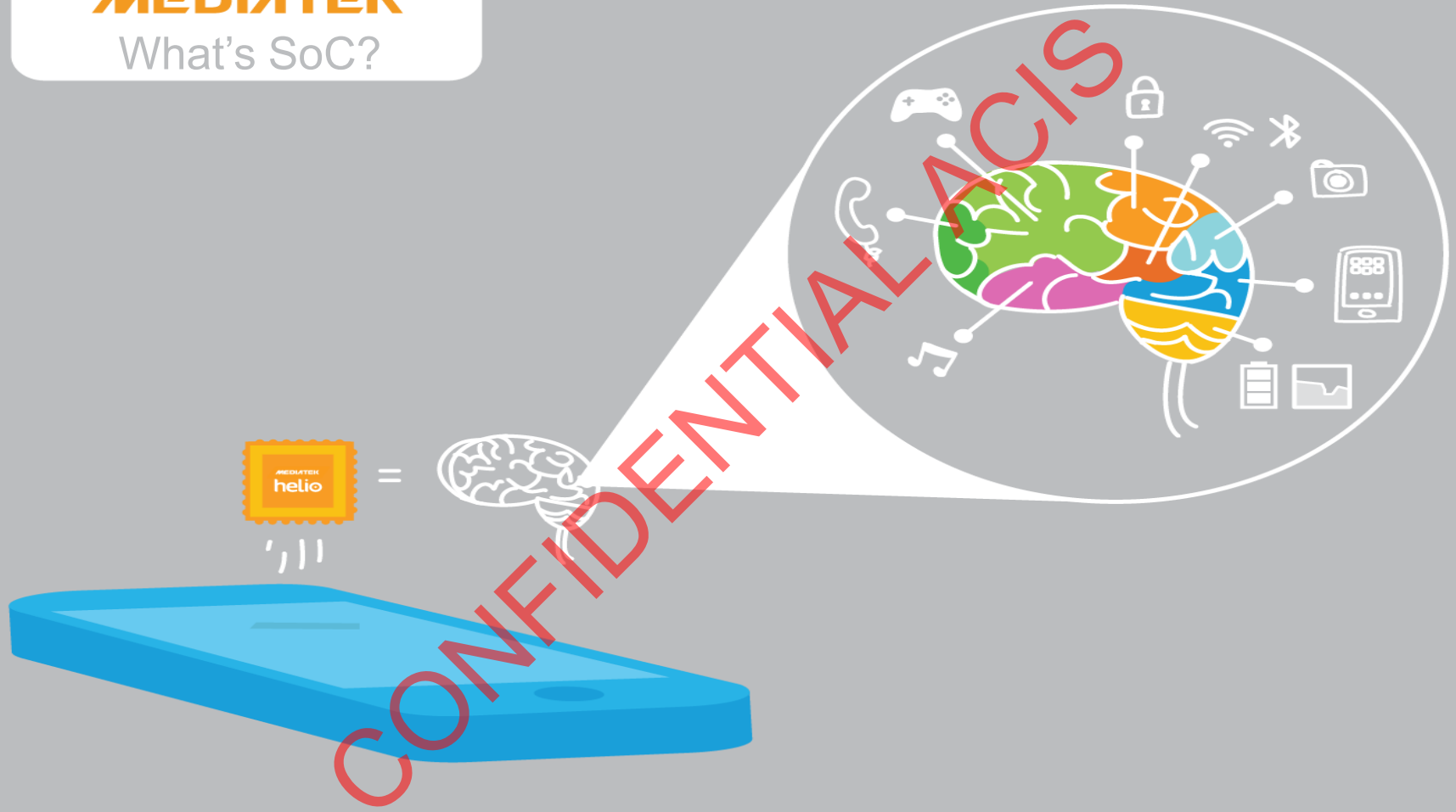


Desempeño Total Superior

Mejor Procesamiento Gráficos

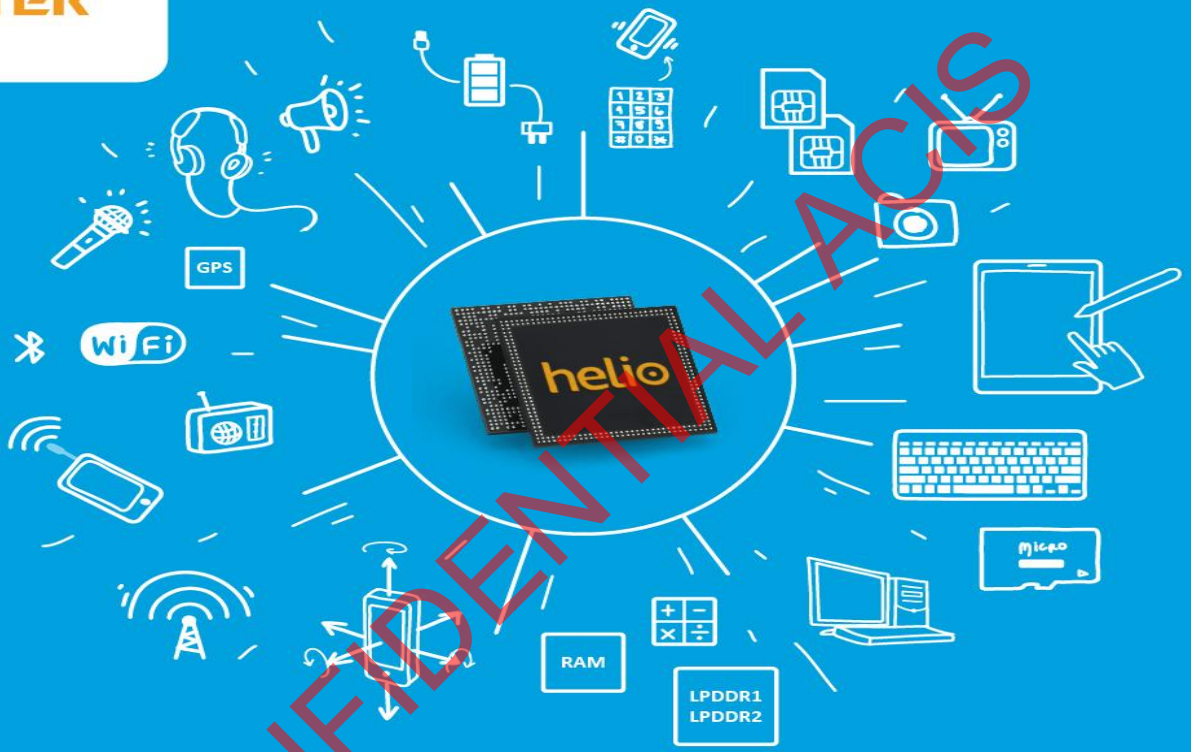
MEDIATEK

What's SoC?



MEDIATEK

helio



Alto desempeño

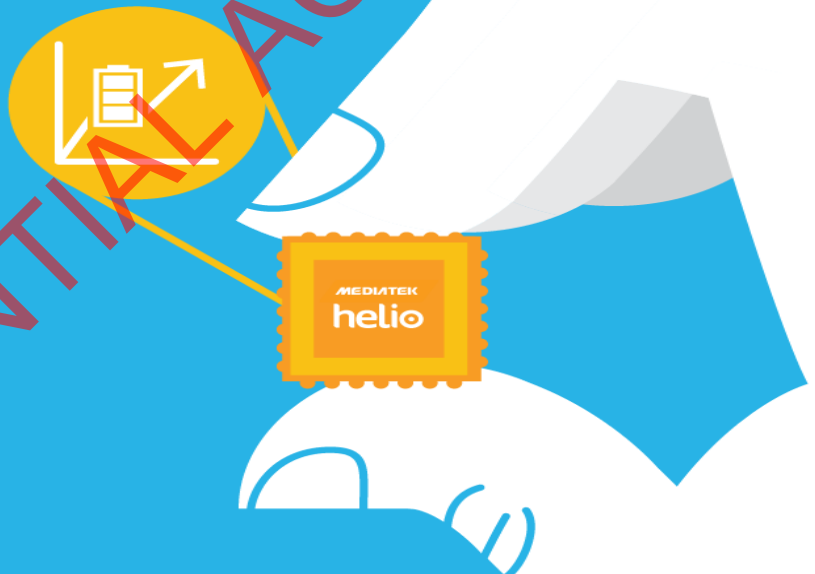
Bajo consumo

Integración

Mayor velocidad

MEDIATEK

What's SoC?

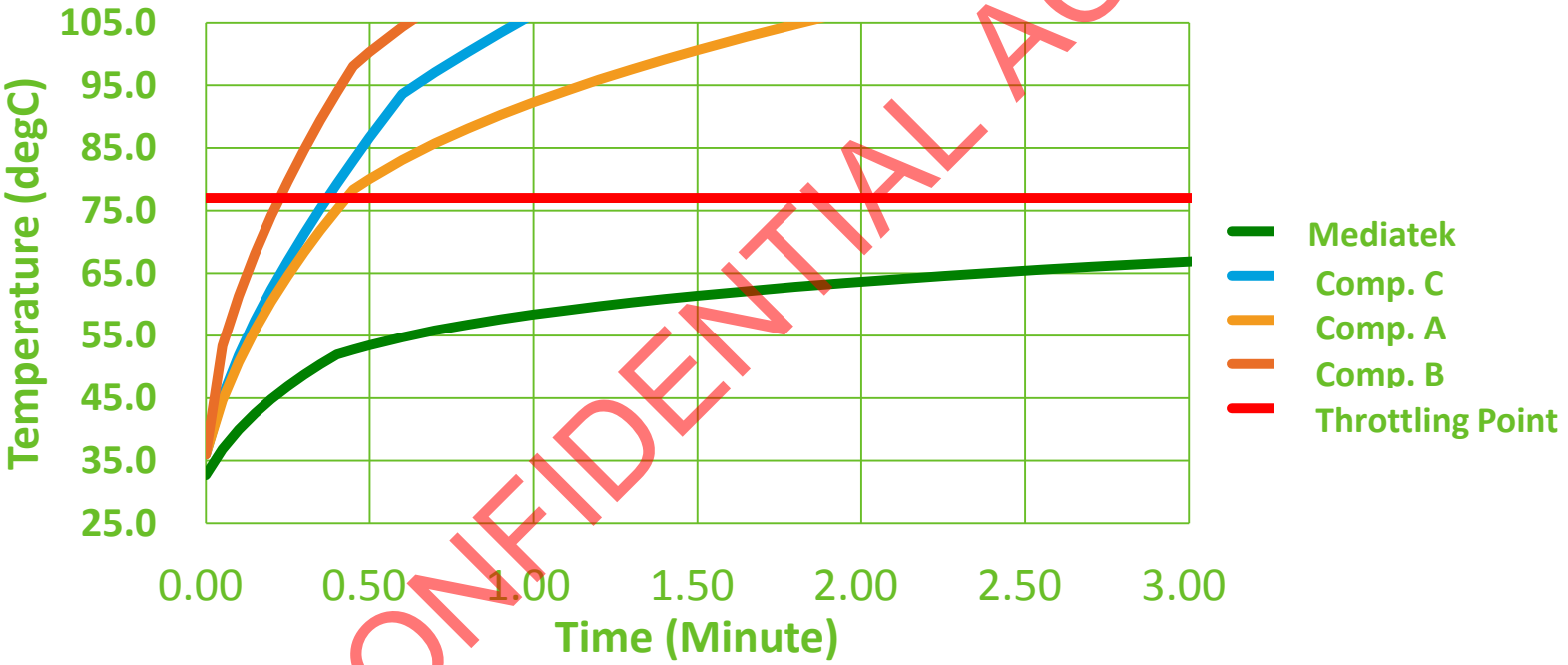


ALTO RENDIMIENTO
BAJO CONSUMO

Desempeño del SoC

Temperatura & el Chipset

Como se enfría un Teléfono?



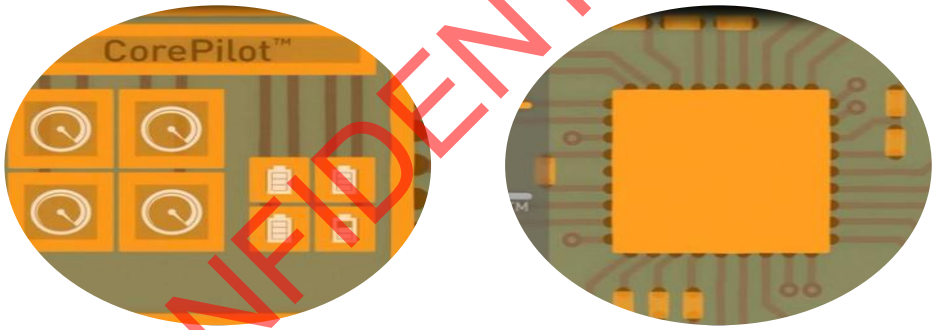
Temperatura del Chipset x tiempo

CORE OR MULTICORE?

QUE SON LOS NUCLEOS? GHZ?

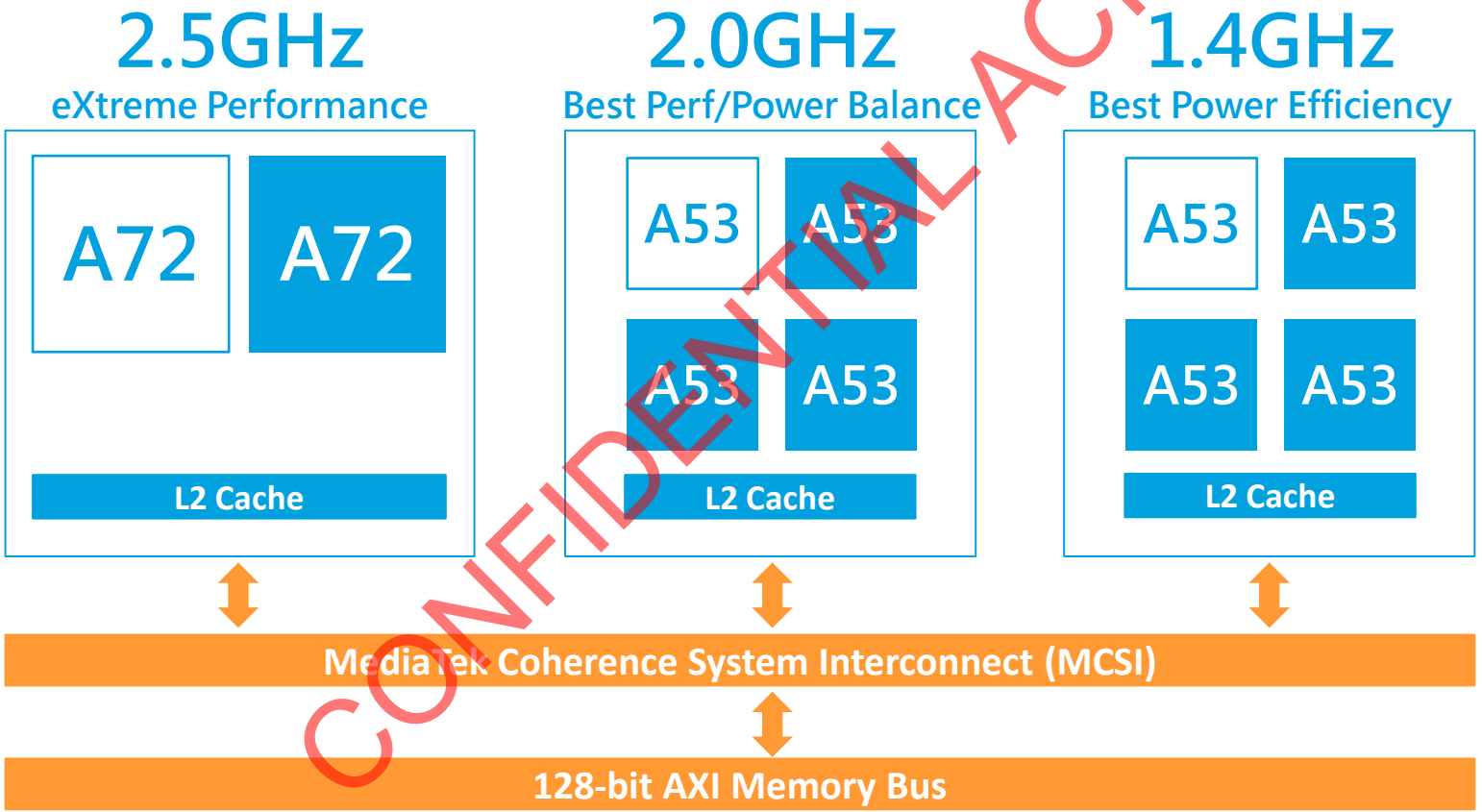
CorePilot™ – Innovation leader

Worldwide 1st HMP Solution	Introduced the first mobile HMP solution on July, 2013
Not just HMP scheduler	A complex architecture to integrate OS kernel scheduler and power components such as ATM and IPM
Outstanding Performance	20% performance uplift and 20% power reduction compared with competitive alternatives



Excellent Framework baseline for CPU and GPU heterogeneous computing

Deca/10-Core CPU Architecture
TRI CLUSTER COMPUTING

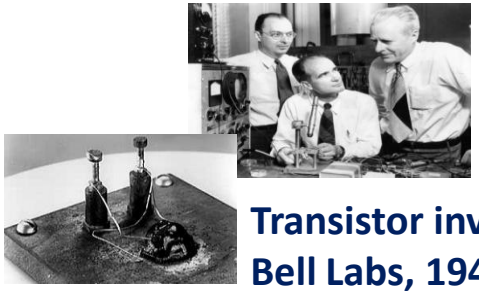


Complexity of IC Design

MediaTek Design Technology

- Functional Unit supporting all Business Units
- Design methodology, flows, tools
- Design services
- Silicon implementation of all products
- 450+ engineers spanning the globe

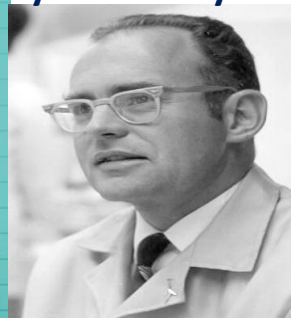
Rise of semiconductor electronics



Transistor invented
Bell Labs, 1947

First integrated circuit
Fairchild Semi, 1960

Gordon Moore, in an 1965 article, observed the steady doubling of integrated electronic devices, year after year …



"Moore's Law"

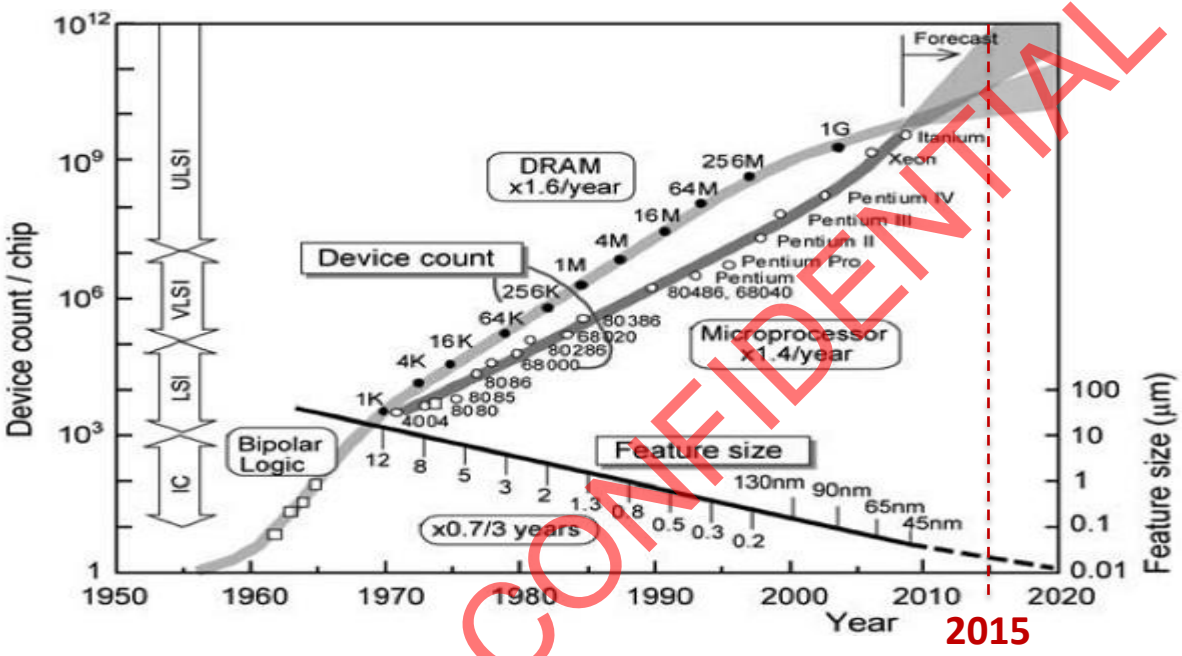
After 50 years of Moore's Law...

Transistor dimension ~10 nm (10^{-9} meter)

~5 billion transistors in a single chip

Cost per transistor ~10^{-9} US $

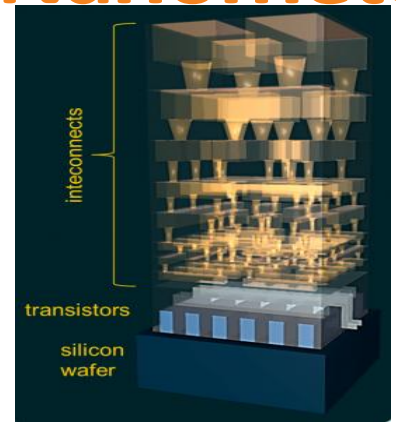
~250,000,000,000,000,000,000 transistors built in 2014

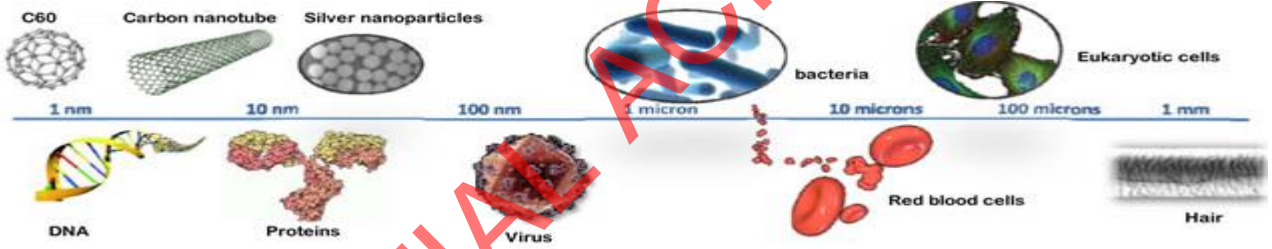


"Frankly, I didn't expect to be so precise."

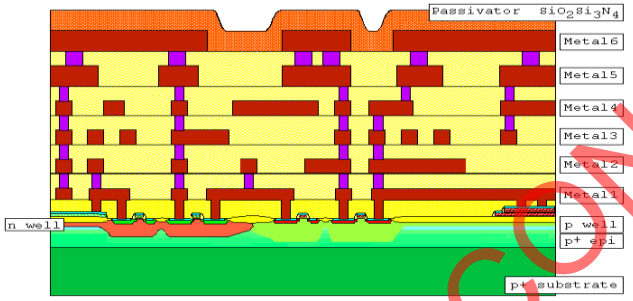
Gordon Moore
Intel co-founder and author of Moore's law

Nanometer scales





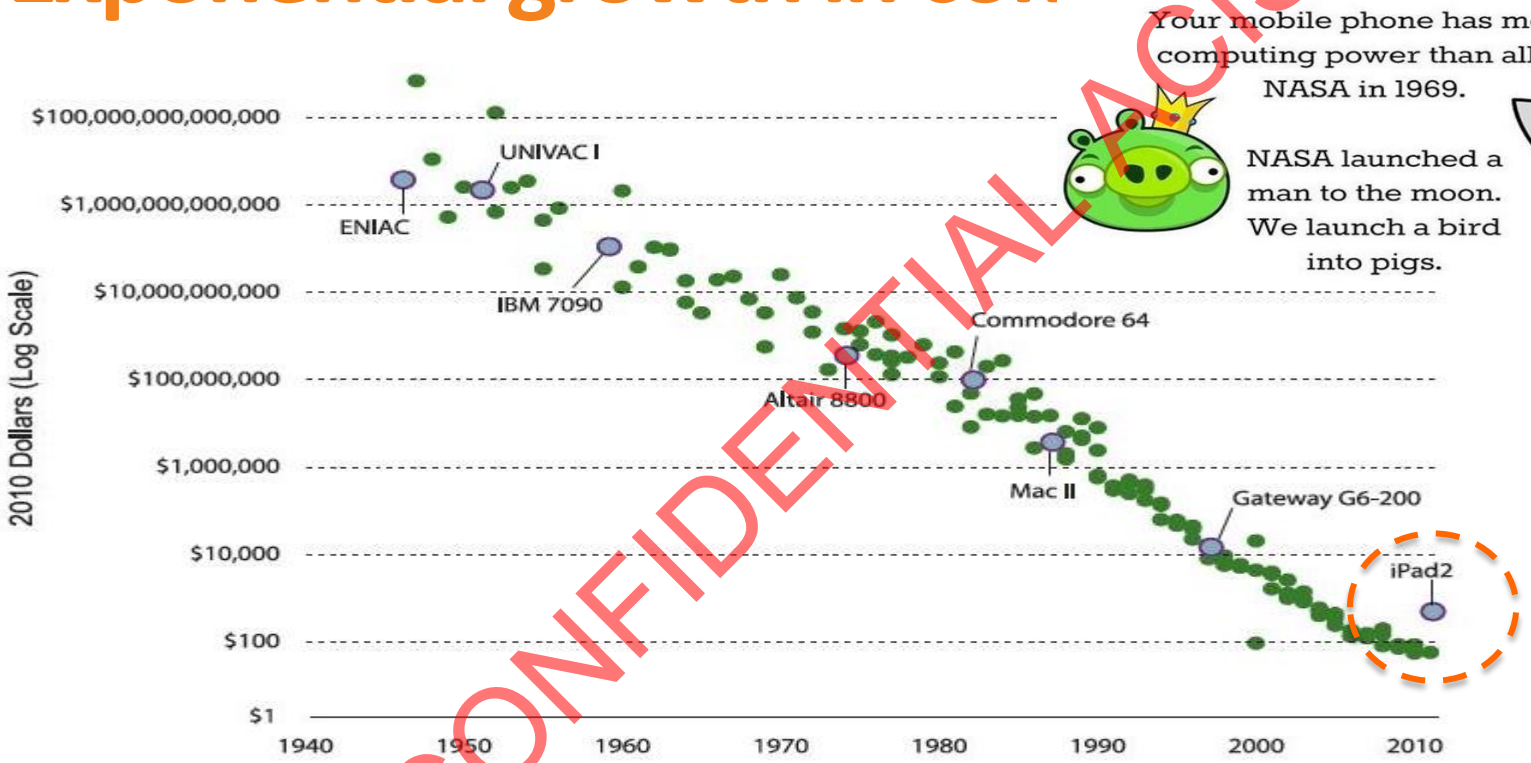
Billions of wire connections!



2014
20 nm feature
2B transistors
100 mm² SoC

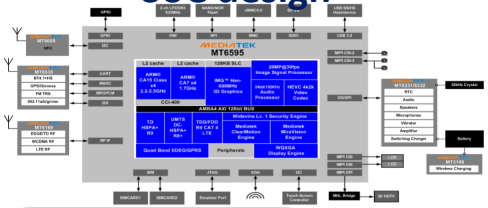
1970, 12 µm feature
2B transistors
36 m² apartment

Exponential growth in computing power

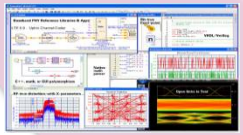


Semiconductor industry eco-system

IP cores, fabless
SoC design



Source: IC Insights



electronic design
automation tools

wafer fab
foundry

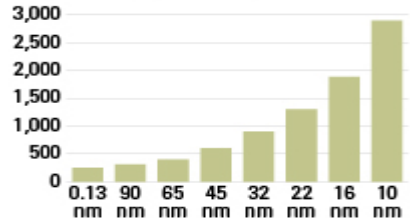
semi
fab
equipment

package, assembly & test

Complex chips are expensive to create

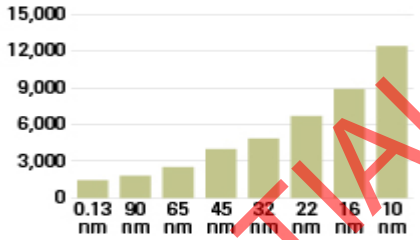
Costs by node (US$ millions)

Process Technology Development



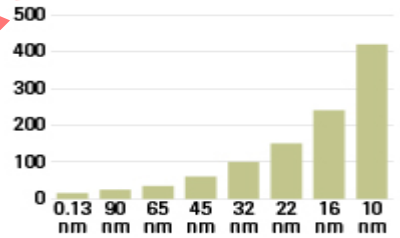
3B

Fab Plant & Equipment

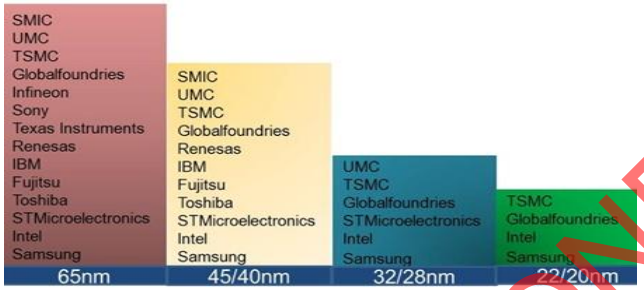


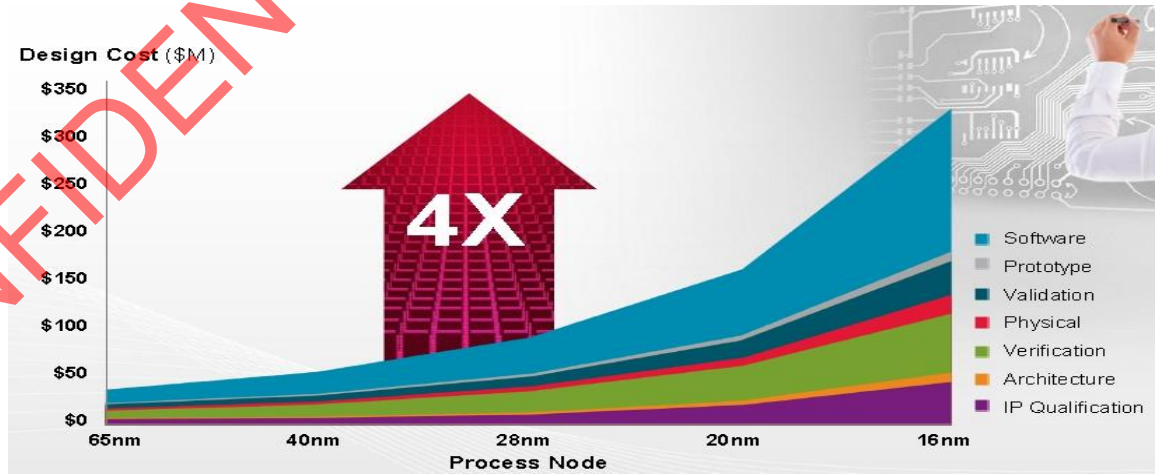
12B

Chip Design



400M





Team of hundreds to design System-on-Chip (SoC)

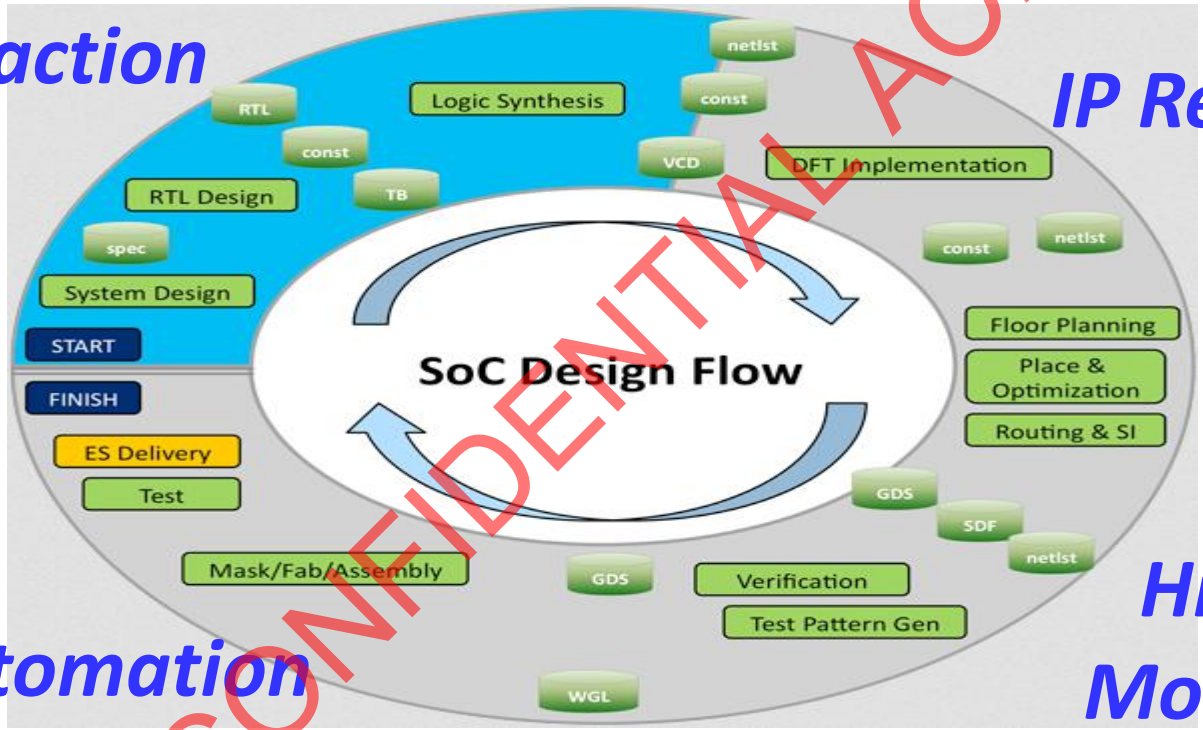
Major Design Concerns

- functionality • functional correctness
- performance • area • power • thermal
- implementation • manufacturability
- testability • product quality
- time-to-market & volume schedule

Managing complexity in SoC design flow

Abstraction

IP Re-use



Automation

Hierarchy

Modularity

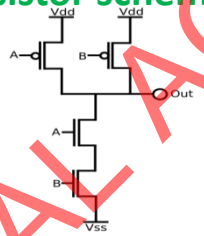
Design at higher levels of abstraction

logic expression

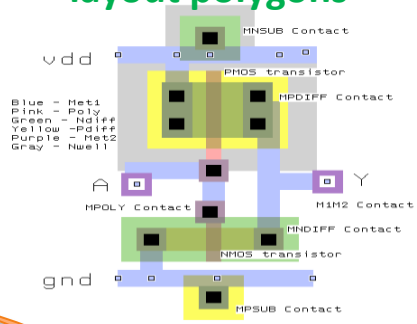
Y = ~(A & B)

logic gate

transistor schematic



layout polygons



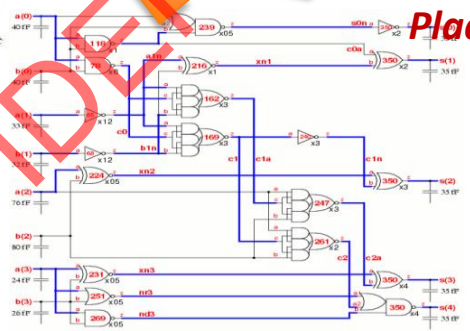
RTL code in HDL

```
// 2. RUN_TEST_IDLE
always @(posedge trst_in or posedge tck_in)
  begin
    if(trst_in)
      run_test_idle <= 1'b0;
    else if (tms_rst1 & tms_rst2 & tms_rst3 & tms_rst4 & tms_rst5)
      run_test_idle <= 1'b0;
    else if (~tms_in & (run_test_idle | test_logic_reset| update_dr
      run_test_idle <= 1'b1;
    else
      run_test_idle <= 1'b0;
  end

// 3. SELECT_DR
always @ (posedge trst_in or posedge tck_in)
  begin
    if(trst_in)
      select_dr <= 1'b0;
    else if (tms_rst1 & tms_rst2 & tms_rst3 & tms_rst4 & tms_rst5)
      select_dr <= 1'b0;
    else if (tms_in & (run_test_idle | update_dr | update_ir))
      select_dr <= 1'b1;
    else
      select_dr <= 1'b0;
  end
```

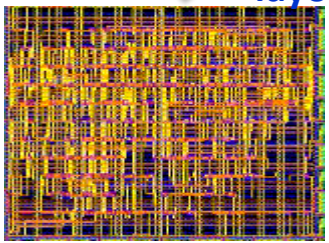
Logic Synthesis Tool

standard cell netlist



Physical Place & route Tool

physical layout

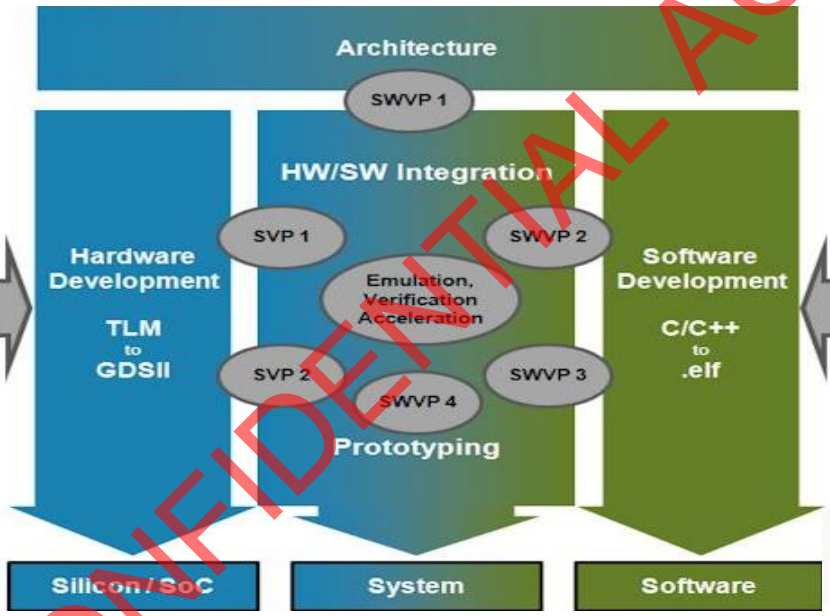


Tools optimize design for area, timing and power constraints

Accelerate system-level design with virtual prototypes

SVP
Silicon Virtual Prototype

- TLM
- System-C
- RTL



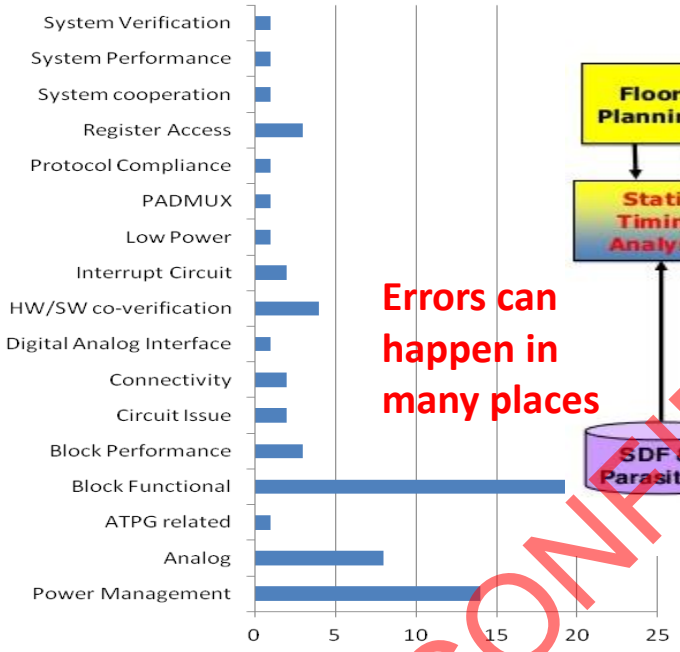
SWVP
Software Virtual Prototype

- C/C++
- Matlab
- Firmware

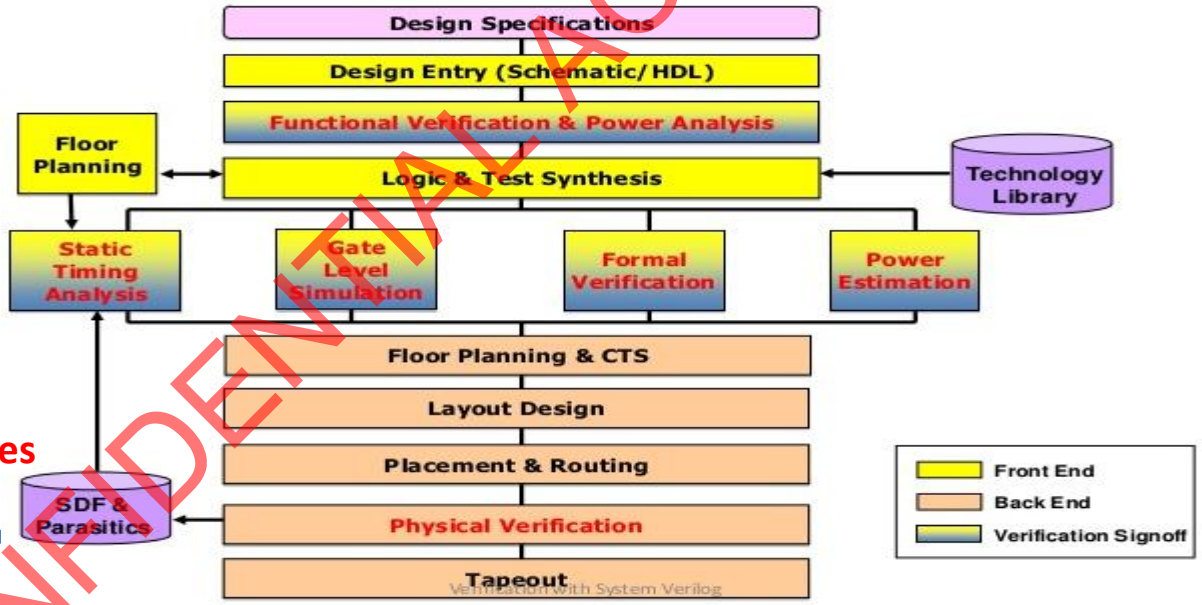
hardware accelerator/emulator

FPGA prototype

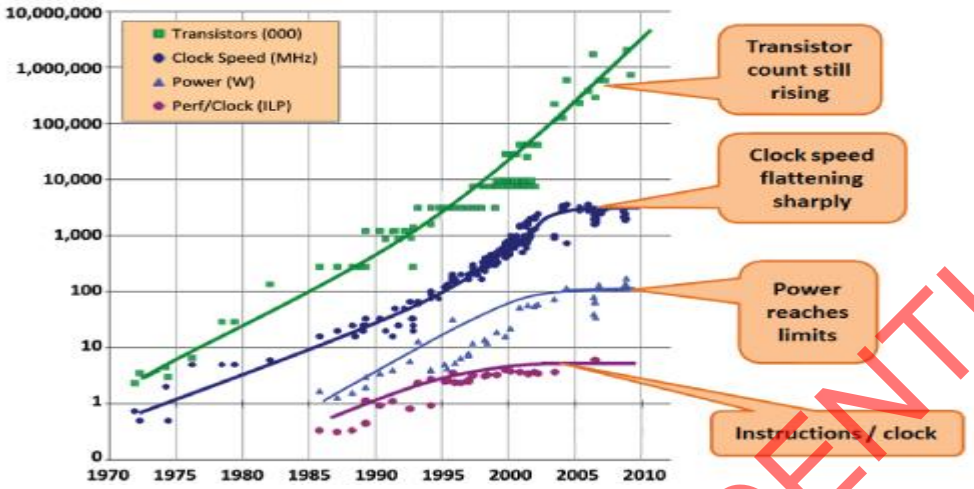
Verification at key checkpoints



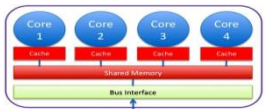
Errors can happen in many places



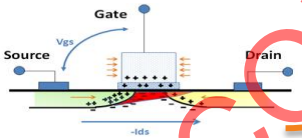
Must consider power in all phases



multiple cores



dark silicon

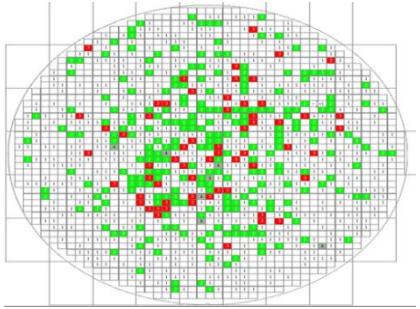


More complex software & hardware

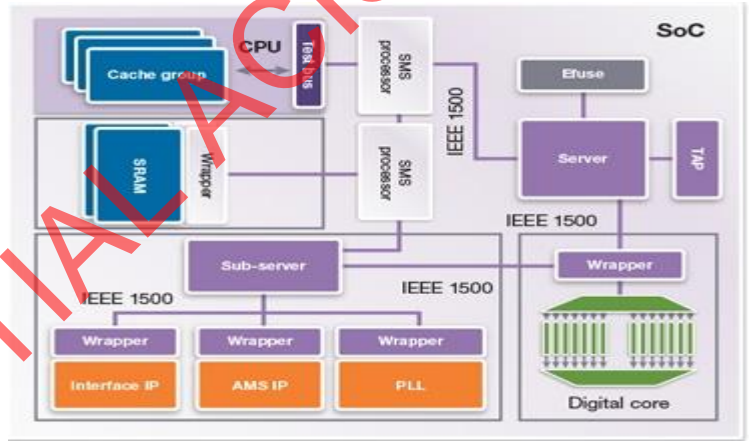
- ❑ Architectural power scenarios
- ❑ Power implementation
- ❑ Power verification

Methodology
Multiple Voltage Islands
Multi-Voltage Supplies (MV)
Lower VDD Operation
MT-CMOS Power Gating
Biasing: Standby/Body
Multi-Vt Optimization (Leakage)
Clock Gating
Clock Tree Synthesis
Channel Length (Multi-Channel)
DVFS/AVS

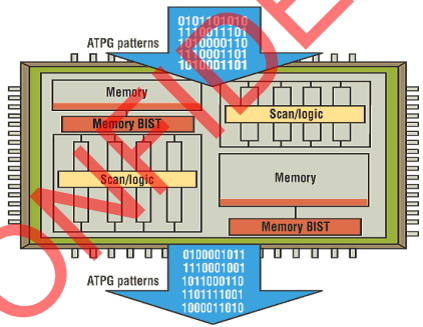
Making sure the design can be tested



Wafer can contain defective dies



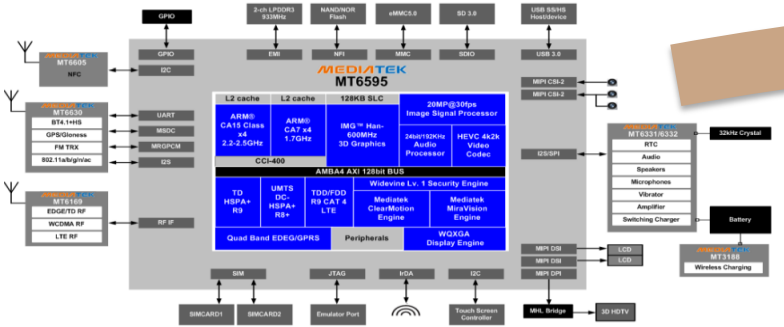
Automatic test pattern generation (ATPG) to minimize test cost & enha...

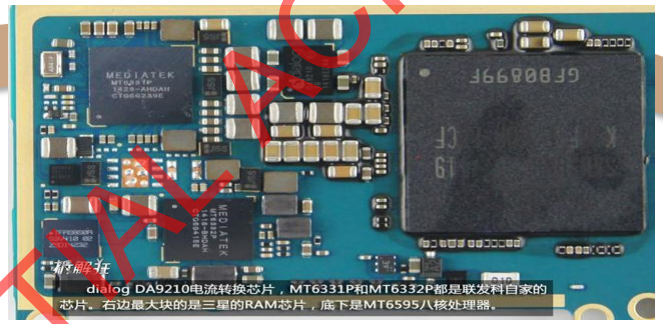


Modular testability architecture and design-for-test (DFT) hardware ensures thorough testing of SoC

Happy customers!

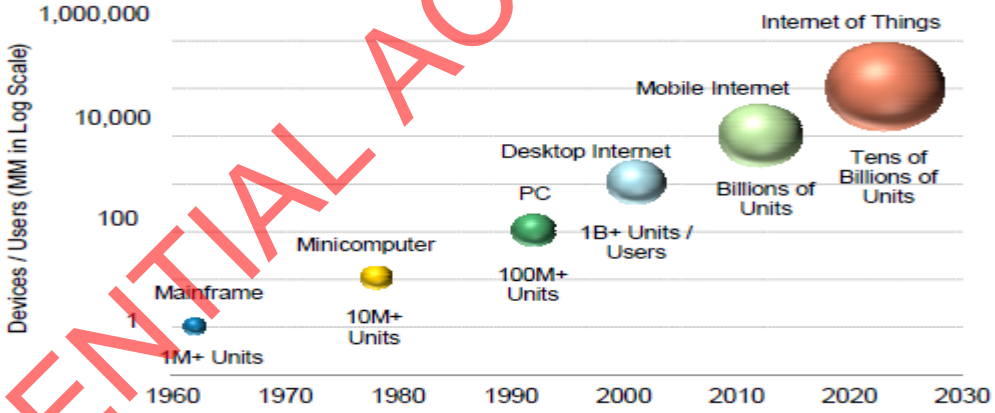
Fantastic end-user experience!

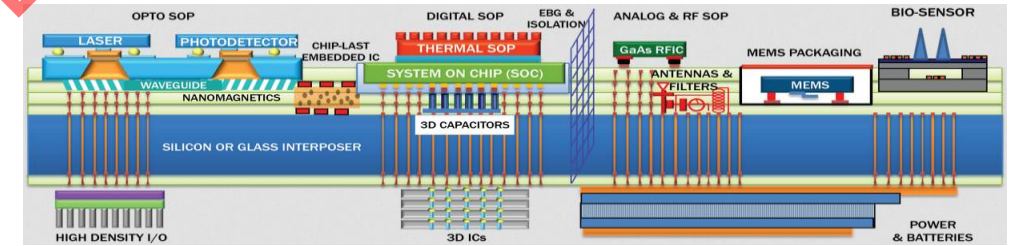




Looking towards the future

Smarter and connected World





Rising new challenges

- Moore's Law will come to an end
- More-than-Moore hetero-integration
- System and app-driven design methods
- System-wide security, reliability, and resilience

everyday genius